The Examiner's objection is not well understood. Registers that perform functions on the stored quantities are well known, i.e. shift registers. A quantum register according to the present invention is well described throughout the specification. For example, quantum registers are explicitly discussed on page 3 line 29 through page 4 line 31, page 5 lines 19 through 25, page 16 line 1 through page 18 line 23, and shown explicitly in Figures 7 and 8. Discussions of the functioning of the components of registers 700 and 800 of Figures 7 and 8, respectively, are presented throughout the entire specification.

Furthermore, the Examiner has a similar rejection with regard to Claim 14, stating that

> Claim 14 shows a register which consists of two banks with intervening islands, with the group being connected with JJs. It is not known how such a structure would form a register and thus the device is not enabling of a register structure.

Again, embodiments of a quantum register are described throughout the specification, as is discussed with Claim 12 above. Therefore, the Examiner's objection is not understood.

Finally, with respect to Claim 15, the Examiner states that

> Claim 15 shows a SET connection between each island and the second bank. It is not known how such a structure would form a register and thus the device is not enabling of a register structure. It is also not shown how to fabricate such a device nor the method of fabricating the SET nor what its structure is.

Again, quantum registers and the function of the described components of embodiments of quantum registers are described through the specification. Furthermore, single electron transistors are discussed on page 15, lines 4-16. As described there, SETs are well known in the field of superconducting devices. Further, production of components, e.g. the quantum cohere, is described in the specification on page 8 lines 4 through 18. As described there, components of quantum registers, e.g. quantum coherers, can be formed with conventional techniques.

The Examiner indicates that "[s]imilar remarks hold for Claims 16, 17, and 18." However, as discussed above, the elements of claims 12-18 are discussed throughout the specification and are enabled. The Examiner is therefore requested to remove the rejections under 35 U.S.C. § 112, first paragraph.

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Rejections of Claims 12-18 under 35 U.S.C. §112, second paragraph

The Examiner has rejected Claims 12-18 "under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which application regards as the invention." In particular, the Examiner states that

> With respect to claim 12 and 14, it is not understood how such a device could function as a register. In particular it is not understood how the SET devices are fabricated or designed and is it [sic] not understood how they would function.

As was discussed above, the elements of Claims 12-18 are described throughout the specification. Further, embodiments of quantum registers are described throughout the specification, as indicated above. Therefore, the Examiner is requested to remove this rejection of Claims 12-18 as well.

Rejections under 35 U.S.C. § 103

Claims 1 and 3-5

The Examiner has rejected Claims 1 and 3-5 "under 35 U.S.C. 103(a) as being unpatentable over Char et al." In particular, the Examiner states that "Char et al. show the formation of grain boundary JJs of high temperature superconductor material (see cover Figures and column 2, line 3 et seq.) where an island 310 is connected to a body 312." However, Char et al. does not teach "a mesoscopic island" as is recited in Claim 1.

Char et al. teaches "a novel and useful method of depositing superconducting film on two sections of a uniform planar substrate to produce a grain boundary weak-link junction at a predetermined location." Char et al., col. 3, lines 21-25. Furthermore, Char et al. teaches formation of weak link Josephson junctions, which "make it possible to create extremely sensitive instruments to measure magnetic field, voltage, and current." Char et al., col. 2, lines 15-17. However, Char et al. does not teach formation of "a mesoscopic island" as is recited in Claim 1. The only teaching of structure size in Char et al. is with Figure 14, where structures of 25 μm or greater are shown. Mesoscopic islands, which have structures of size such that a single excess Cooper pair is noticeable, is of size much smaller than those taught in Char et al.

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Claims 3-5 depend from Claim 1 and are therefore allowable over Char et al. for at least the same reasons as is Claim 1.

Claim 2

Claim 2 has been "rejected under 35 U.S.C. 103(a) as being unpatentable over Char et al. in view of Shnirman et al." In particular, the Examiner states that

> Char et al. show the basic device and Shnirman et al. show the use of a SET to read out a JJ q-bit (see Figure 1 and page 57, second column et seq.). It would have been obvious to modify the Char et al. device to include the SET to provide a readout for the Char et al. device.

As discussed above, Claim 1 is allowable over Char et al. Shnirman et al. does not make up the difference. Furthermore, there is no motivation to combine Char et al. with Shnirman et al. since Char et al. teaches relatively large superconducting structures for precise measurement of voltages, magnetic fields, and currents whereas Shnirman et al. teaches to "measure the quantum state by coupling a single-electron transistor to [a] qubit." Shnirman et al., abstract. Furthermore, the SET of Claim 2 recites that the SET is "connected between the island and ground" and does not imply that the SET is only a readout mechanism.

Claim 2, therefore, is allowable over the combination of Char et al. and Shnirman et al.

Claims 6 and 8-10

Claims 6 and 8-10 "are rejected under 35 U.S.C. 103(a) as being unpatentable over Char et al. in view of Baechtold et al." In particular, the Examiner states that

> Baechtold et al. show a binary circuit consisting of a series/parallel arrangement of JJs (see Figure 4 and column 5, line 57 et seq.). It would have been obvious to use the Char et al. structure in the Baechtold et al. device to provide the JJs.

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Claim 6 depends from Claim 1. Claim 1 is allowable over Char et al. as discussed above. Baechtold et al. does not make up the difference. Therefore, Claim 6 is allowable over Char et al. in combination with Baechtold et al.

Claim 8 recites "a plurality of mesoscopic islands . . . ." As discussed above with respect to Claim 1, Char et al. does not teach a "mesoscopic island." Baechtold et al. does not make up the difference. Therefore, Claim 8 is allowable over Char et al. in combination with Baechtold et al. Claims 9 and 10 depend from Claim 8 and are therefore allowable for at least the same reasons as is Claim 8.

Claims 7, 11 and 12-18

Claims 7, 11 and 12-18 were "rejected under 35 U.S.C. 103(a) as being unpatentable over Char et al. in view of Baechtold et al. and further in view of Shnirman et al." The Examiner states that "[w]ith respect to claims 7 and 11, It [sic] would have been obvious to use the Shnirman et al. structure to provide a readout for the device." Further, the Examiner states that "[w]ith respect to claims 12-18, it would be obvious to apply the structures described above in various combinations since the basic combination is shown."

Claim 7 depends from Claim 1. As discussed above, Claim 1 is allowable over Char et al. and Baechtold et al. and Shnirman et al. do not make up the difference. Therefore, Claim 7 is allowable for at least the same reasons as is Claim 1.

Claims 11-18 depend from Claim 8. As discussed above, Claim 8 is allowable over Char et al. and Baechtold et al. and Shnirman et al. do not make up the difference. Therefore, Claims 11-18 are allowable for at least the same reasons as is Claim 8.

New Claims

Claims 28 through 51 have been added to the present application. Claims 28 through 51 are allowable over the cited art.

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Conclusion

Claims 1-18 are pending in the above identified application. Claims 1, 8, 9, 13, and 18 have been amended and Claims 28-51 have been added. Applicants believe that Claims 1-18 and 28-51 are allowable and therefore request that the Examiner issue of Notice of Allowability on Claims 1-18 and 28-51. If other than a Notice of Allowability is contemplated, the Examiner is invited to contact Applicants' attorney by email at gedwards@skjereven.com or by phone at (408)453-9200 ext. 1338.

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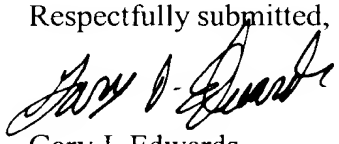
Respectfully submitted,



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Appendix of Amendments

(Additions are presented as underlined and deletions are presented in [brackets])

In the Specification

On Page 2, the paragraph starting with line 8 is replaced with:

Quantum computing generally involves initializing the states of N qubits (quantum bits), creating controlled entanglements among the N qubits, allowing the quantum states of the qubits to evolve under the influence of the entanglements, and reading the qubits after they have evolved. A qubit is conventionally a system having two degenerate quantum states, and the initial state of the qubit typically has non-zero probabilities of being found in either degenerate state. Thus, N qubits define an initial state that is a combination of 2^N degenerate states. The entanglements control the evolution of the distinguishable quantum states and define calculations that the evolution of the quantum states [performs]perform. This evolution, in effect, performs 2^N simultaneous calculations. Reading the qubits after evolution is complete determines the states of the qubits and the results of the calculations.

On Page 3, the paragraph starting on line 22 is replaced with

To read the supercurrent state associated with the island, a single electron transistor (SET) or parity key can connect the island to ground. When the SET is biased to conduct, the current through the SET collapses supercurrent state to a [state]states with fixed magnetic moment and fixes the supercurrent in that state. Thus, upon completion of a calculation, a control circuit biases the SET to conduct, and the magnetic moment at the Josephson junction is fixed in a particular state and can be dependably read.

On Pages 12 and 13, the paragraph starting on line 23 of Page 12 is replaced with

Figs. 4A and 4B respectively show plan and cross-sectional views of a quantum coherer 400 having a vertical architecture according to another embodiment of the invention. Quantum coherer 400 includes a superconductor bank 410, a mesoscopic superconductor island 420, and a Josephson junction 430, formed on an insulating substrate 440. A fabrication process for quantum coherer 400 grows a d-wave superconductor film on substrate 440 to a thickness less than about 0.2 μm and patterns the film to form island 420. Insulative sidewall spacers 450 are then formed on island 420. Such spacers can be conventionally formed by depositing and patterning an insulative layer or by [as]a self-aligned process that anisotropically etches a conformal insulative layer formed on substrate 440 and island 420. A layer of a normal conductor such as gold is deposited on the resulting structure to a thickness between about 0.1 μm and about 0.3 μm and patterned to form a normal conductive region of Josephson junction 430. The normal conductive region extends over island 420 and at least part of sidewall spacers 440. Finally, a layer of an s-wave superconductor is deposited on the structure and patterned (if necessary) to form bank 410. The thickness of bank 410 is not critical to the operation of quantum coherer 400.

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On Page 13, the paragraph between lines 9 and 26 is replaced with

Fig. 5 shows a cross-sectional view of a quantum coherer 500 having a hybrid vertical/horizontal architecture according to another embodiment of the invention. Quantum coherer 500 includes a superconductor bank 510, a mesoscopic superconductor island 520, and a Josephson junction 530, formed on an insulating substrate 540. A fabrication process for quantum coherer 500 grows a d-wave superconductor film on substrate 440 to a thickness less than about 0.2 μm and patterns the film to form island 520. The patterning can leave sides of island 520 perpendicular to the surface of substrate 540 or any desired angle. A layer of a normal conductor such as gold is deposited on the resulting structure to a thickness between about 0.1 μm and about 0.3 μm and patterned to form a normal conductive region of Josephson junction 530. In this embodiment, the normal conductive region extends over island 520 and is in contact with at least one sidewall of island 520. Finally, a layer of an s-wave superconductor is deposited on the structure and patterned (if necessary) to form bank 510. The phase difference in the superconducting order parameter from bank 510 to island 520 depends on the relative crystal orientation between the top surface of island 520 and the overlying part of bank 510 and the relative crystal orientation of the side of island [120]520 and the adjacent part of bank 510.

In the Claims

1. (Amended) A quantum computing structure comprising:
a first bank of a superconducting material having a first crystal orientation;
[an]a mesoscopic island of a superconducting material having a second crystal orientation, wherein at least one of the island and the bank comprises a d-wave superconducting material; and
a clean Josephson junction between the island and the bank.

8. (Amended) A quantum register comprising:
a bank of a superconducting material;
a plurality of mesoscopic islands of superconducting material; and
a plurality of clean Josephson junctions, each clean Josephson junction being between the bank and a corresponding one of the islands.

9. (Amended) The quantum register of claim 8, wherein each of the mesoscopic islands comprises a d-wave superconductor.

13. (Amended) The quantum register of claim 12, further comprising a second plurality of single electron transistors, each single electron transistor in the second plurality being between ground and a corresponding one of the plurality of mesoscopic islands.

18. (Amended) The quantum register of claim 17, further comprising a third plurality of single electron transistors, each single electron transistor in the third plurality being between ground and a corresponding one of the plurality of mesoscopic islands.

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